REMARKS

Claims 1, 3-5, 8-10, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 5,648,793) in view of Moon (US 5,825,343) and Wada (JP 01-106,017) and further in view of Asada (US 5,867,141). Applicant respectfully disagrees.

Independent claim 1 recites a method of driving a liquid crystal display panel of dot inversion system including, in part, "a first input line supplied with a pre-gate start pulse and a second input line supplied with a data output enable signal (DOE) for controlling data output of a data driving integrated circuit, wherein the data driving integrated circuit applies data to the data lines in response to the data output enable signal ... first delay means for delaying the pre-gate start pulse from the first input line by one clock interval of the data output enable signal in response to the data output enable signal; second delay means for delaying the delayed pre-gate start pulse from the first delay means by one clock interval of the data output enable signal in response to the data output enable signal," (emphasis added).

Similarly, independent claim 5 recites a driving apparatus for liquid crystal display panel of dot inversion including, in part, "a data driving integrated circuit supplying data to the data lines of the liquid crystal display panel in response to a data output enable signal (DOE) ... first delay means for delaying the pre-gate start pulse from the first input line by one clock interval of the data output enable signal in response to the data output enable signal; second delay means for delaying the delayed pre-gate start pulse from the first delay means by one clock interval of the data output enable signal in response to a data output enable signal," (emphasis added).

Similarly, independent claim 10 recites a device for driving a liquid crystal display panel

including, in part, "a data driving integrated circuit supplying data to the data lines in response to a data output enable signal (DOE) ... first delay means for delaying the pre-gate start pulse from the first input line by one clock interval of the data output enable signal in response to the data output enable signal; second delay means for delaying the delayed pre-gate start pulse from the first delay means by one clock interval of the data output enable signal in response to a data output enable signal," (emphasis added).

Page 2 of the Office Action alleges that Wada discloses a data output enable signal causing the data driving circuit to apply data to the data lines because "[t]he operation of the polarity switching circuit directly affects the driving signal generating circuit." Applicant understands the Office Action to be suggesting that the output signal from the polarity switching circuit 9 of Wada is the "data output enable signal," as claimed. Applicant respectfully disagrees. The Abstract of Wada discloses that the "polarity switching circuit 9 generates a signal for switching the polarity of the liquid crystal driving voltage." Applicant respectfully asserts that Wada is silent as to the output of the polarity switching circuit 9 being a data output enable signal, as claimed.

Assuming, *arguendo*, that the signal from the polarity switching circuit 9 of Wada is the "data output enable signal," as claimed, Applicant respectfully asserts that the output signal is input only to an Exclusive OR gate and not the driving signal generating circuit 8 of Wada. In particular, the Abstract of Wada discloses that the polarity switching circuit 9 and the driving signal generating circuit 8 of Wada are connected because the polarity switching circuit 9 generates a signal for switching the polarity of the liquid crystal driving voltage with a signal

from a driving signal generating circuit 8," (emphasis added). In other words, the output signal from the polarity switching circuit 9 does not "directly affect" the driving signal generating circuit 8, as alleged by the Office Action.

In addition, the Office Action suggests that the left flip-flop 10 in FIG. 2 of Wada is the "first delay means," as claimed and that the right flip-flop 10 in FIG. 2 of Wada is the "second delay means," as claimed. In contrast to the claimed invention, left and right flip-flops 10 of Wada are provided with delayed signal from the frequency dividing circuit 7. Accordingly, Wada fails to teach or suggest that a DOE signal is supplied to the left and right flip-flops 10.

Applicant respectfully asserts that the applied prior art of record fails to remedy the deficiencies of Wada. Accordingly, Applicant respectfully asserts that the applied prior art references, whether taken singly or combined, fail to teach or suggest the combination of features recited by the independent claims 1, 5 and 10, and hence dependent claims 3, 4, 8, 9, 12, and 13.

CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully requests the reconsideration and the timely allowance of the pending claims. Should the Examiner believe that there are any issues outstanding after consideration of this response, the Examiner is invited to contact Applicant's undersigned representative to expedite prosecution.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. § 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

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